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10/090,250	03/01/2002	Suresh M. Menon	X-1050 US	4098

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,250	MENON ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-16 and 18-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-16 and 18-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The indicated allowability of claim 1-7, 9-16, and 18-19 are withdrawn in view of the newly discovered reference(s) to US 6,091,962. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 20-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

- With regard claim 20, the limitation "wherein each serializer is configurable to transmit data at one of at least two bit rates, and each deserializer is configurable to receive data at one of at least two bit rates" as recited has not been taught in the specification. The specification only teaches "A configuration option of serializer 158 is to transmit 20 bits (high speed) or 10 bits (low speed) of data per reference clock cycle." In paragraph 23 and "A configuration option of deserializer 174 is to receive 20 bits (high speed) or 10 bits (low speed) of data per clock cycle." in paragraph 24 as recited.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 9, 11, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kean (US 5,701,091) in view of Bonta (US 6,091,962).

- With regard claim 1, Kean discloses an integrated circuit comprising:

  a plurality of configuration memory cells (Fig.3 element Switch 15 and column 2 lines 5-19);

  at least one transceiver (Fig.3 elements 78 and 79 and column 1 line 60 – column 2 line 4) containing components having selectable values (Fig.3 elements EN, PUP, RPUP, TPUP, SLEW, OUT), said components being configured by said plurality of configuration memory cells (column 1 line 60 – column 2 line 19).

  Kean discloses all of the subject matter as described in the above paragraph except for specifically teaching wherein one of said components is a loss of synchronization detector.

  However, Bonta teaches that a transceiver with one of components is a loss of synchronization detector (Fig.4 element 52 and column 6 lines 24-48). It would have been obvious to one having ordinary skill in the art at the time the

invention was made to integrate the loss of synchronization detector in a chip with a transceiver in order to discrease the discrete component in a circuit board to shorten the signal path between the transceiver and the loss of synchronization detector so that the synchronization quality can be improved, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art.

- With regard claim 9, Kean further discloses a programmable fabric (Fig.1 and column 1 lines 14-40); and

at least one signal generated by said programmable fabric for controlling said values of said components (Fig.3 elements 15-18).

- With regard claim 11, Kean discloses an integrated circuit comprising:

a programmable fabric (Fig.1 and column 1 lines 14-40);

a processor core surrounded by said programmable fabric (column 1 lines 28-40 and column 3 lines 23-38);

a plurality of configurable transceivers located at the peripheral of said programmable fabric (Fig.3 elements 78 and 79 and column 1 line 60 – column 2 line 4); and

a plurality of signal paths connecting at least one of said configurable transceivers and said processor core, at least a portion of each of said signal paths passing through said programmable fabric (Fig.3 elements 15-18, Switching output EN, OUT, PAD IN and column 1 line 52 – column 2 line 19).

Kean discloses all of the subject matter as described in the above paragraph except for specifically teaching wherein one of said components is a loss of synchronization detector.

However, Bonta teaches that a transceiver with one of components is a loss of synchronization detector (Fig.4 element 52 and column 6 lines 24-48). It would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the loss of synchronization detector in a chip with a transceiver in order to discrease the discrete component in a circuit board to shorten the signal path between the transceiver and the loss of synchronization detector so that the synchronization quality can be improved, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art.

- With regard claim 12, all limitation is contained in claims 11 and 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 18, Kean further discloses wherein said programmable fabric generates at least one signal for controlling at least one of said configurable transceivers (Fig.3 elements 15 output EN, OUT and PAD IN and column 1 line 52 – column 2 line 19).

6. Claims 2-5, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kean (US 5,701,091) and Bonta (US 6,091,962) as applied to claim 1 above, and further in view of Plants (US 6,237,124).

- With regard claim 2, Kean and Bonta disclose all of the subject matter as described in the above paragraph except for specifically teaching one of said components is a cyclic redundancy code generator.

  However, Plants teaches a cyclic redundancy code circuit generator (Fig.4 element 40 and column 7 line 1 – column 8 line 37) in an integrated circuitry or FPGA. It is inherent that the FPGA contains an I/O circuitry with a transceiver, driver for output signal and receiver for input signal (column 4 line 64 – column 5 line 4).

  It is desirable to have a cyclic redundancy code circuit generator in an integrated circuitry or FPGA to indicate an error has occurred during signal processing operation and take necessary action to correct the error so as to improve the FPGA operation performance. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include circuit as taught by Plants in which having a cyclic redundancy code circuit generator in an integrated circuitry, into Kean and Bontas' integrated circuit so as to improve the FPGA operation performance.

- With regard claim 3, Kean and Bonta disclose all of the subject matter as described in the above paragraph except for specifically teaching one of said components is a cyclic redundancy code verification block.

  However, Plants teaches a cyclic redundancy code circuit verification block (Fig.4 element 40 and column 7 line 1 – column 8 line 37) in an integrated circuitry or FPGA.

It is desirable to have a cyclic redundancy code circuit verification block in an integrated circuitry or FPGA to verify and indicate an error has occurred if the known correct values do not match with the signature during signal processing operation and take necessary action to correct the error so as to improve the FPGA operation performance. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include circuit as taught by Plants in which having a cyclic redundancy code circuit verification block in an integrated circuitry, into Kean and Bontas, integrated circuit so as to improve the FPGA operation performance.

- With regard claims 4 and 5, Kean and Bonta disclose all of the subject matter as described in the above paragraph except for specifically teaching one of said components is a serializer/ deserializer.

However, Plants teaches a serializer/ deserializer (Fig.4 element 32 and column 5 lines 10-25) in an integrated circuitry or FPGA. Note that, Upon either power up or at device reset, an EPROM controller 32 *serializes* the data stream from the EPROM 30 into a serial data stream (SDATA) one bit wide. Inherently, the EPROM controller 32 will *deserializes* the data stream to the EPROM 30. It is desirable to have a serializer/ deserializer in an integrated circuitry or FPGA to reduce the number of pins in a integrated circuit in order to improve the manufacturing ability such as soldering when the IC is mounted in a print circuit board. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include circuit as taught by Plants in which having a serializer/ deserializer in an integrated circuitry, into Kean and Bontas'

integrated circuit so as to improve the manufacturing ability such as soldering when the IC is mounted in a print circuit board.

- With regard claim 13, all limitation is contained in claims 10, 3, and 2. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 14, all limitation is contained in claims 10, 5, and 4. The explanation of all the limitation is already addressed in the above paragraph.

7. Claims 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kean (US 5,701,091), Bonta (US 6,091,962) and Plants (US 6,237,124) as applied to claims 5 and 10 above, and further in view of Schneider (US 6,594,275).

- With regard claim 6, Kean and Bonta and Plants disclose all of the subject matter as described in the above paragraph except for specifically teaching the deserializer further comprises configurable comma detection function.

  However, Schneider teaches a deserializer with comma detection function (Fig.1 element 12, column 6 lines 12-17, column 7 lines 8-38, and column 8 lines 15-21).

  It is desirable to have a deserializer with comma detection function. The reason for this is that the serial in, parallel out shift register in an integrated circuit is typically large enough-to capture an entire byte-multiple word of data, to facilitate the detection of a delimiter character (i.e., a character such as a comma which facilitates the proper framing of the data as byte-multiple parallel data words), so that the data conversion processing performance is improved. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the function as taught by Schneider in

which having a deserializer with comma detection function, into Kean and Bonta and Plants' integrated circuitry so as to improve the data conversion processing performance.

- With regard claim 15, all limitation is contained in claims 10 and 6. The explanation of all the limitation is already addressed in the above paragraph.

8. Claims 7, 10, 16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kean (US 5,701,091) and Bonta (US 6,091,962) as applied to claims 1, 9, 12, and 18 above, and further in view of Hausman et al. (US 5,872,920).

- With regard claim 7, Kean and Bonta disclose all of the subject matter as described in the above paragraph except for specifically teaching one of said components is an elastic buffer.

  However, Hausman et al. teaches an elastic buffer in an integrated circuitry (Fig.1 element 210, 160, 170, 080, and 190, and column 2 lines 24-60).

  It is desirable to have an elastic buffer in an integrated circuitry to control and adjust the input and output packages so that the data overflow issue is improved. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the circuit as taught by Hausman et al. in which having an elastic buffer in an integrated circuitry, into Kean and Bontas' integrated circuit so that the data overflow issue is improved.

- With regard claim 10, Kean and Bonta disclose all of the subject matter as described in the above paragraph except for specifically teaching one of said components is an encoder, and said at least one signal controls said encoder.

However, Hausman et al. teaches an encoder (Fig.1 element 120 and column 2 lines 34-40) in an integrated circuitry (Fig.1 element 210 and column 2 lines 49-60) and said at least one signal controls said encoder (Fig.1 elements 120 and 140 and column 2 lines 34-60).

It is desirable to have an encoder in an integrated circuitry to provide an encoded signal with proper package length to external device and said at least one signal controls said encoder to control the speed of the encoder output in order to adjust the encoded output packages so that the data overflow issue is improved. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the circuit as taught by Hausman et al. in which having an encoder in an integrated circuitry to provide an encoded signal to external device and said at least one signal controls said encoder, into Kean and Bontas' integrated circuit so that the data overflow issue is improved.

- With regard claim 16, all limitation is contained in claims 7 and 12. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 19, all limitation is contained in claims 10 and 18. The explanation of all the limitation is already addressed in the above paragraph.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang

KEVIN BURD
PRIMARY EXAMINER